



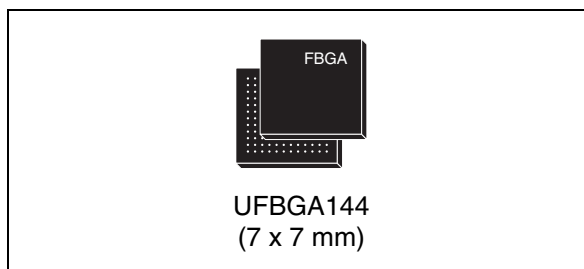
STM32TS60

Multitouch screen controller device using a digital resistive touchpanel with I²C, SPI, UART and USB interfaces

Data brief

Features

- Patented digital resistive multitouchpanel technology powered by Pmatrix™ firmware engine
- Able to track up to 10 independent touches simultaneously
- Finger, nail and any stylus touch capability
- Up to 0.17 mm resolution
- Touch actuation force information
- No calibration requirements
- Typical touchpanel scan rate of 125 Hz up to 250 Hz
- Single- or dual-chip architecture able to support up to 10.1" screens
- Single-chip controller able to support up to 129 rows/columns coming from the sensor matrix.
- Embedded compensation resistors for reduced BOM and easy connection to the touchpanel
- I²C, SPI, UART and USB communication interfaces
- Very low power mode allowing "wakeup on touch/release" mode
- Wakeup response time: 10 µs from Sleep mode and 100 µs from Standby mode



Applications

- Gaming devices
- Mobile handsets
- Smart phones
- Portable media players
- Personal navigation devices
- Mobile internet devices
- Netbooks

Table 1. STM32TS60 device summary

Feature	Description
Touchpanel size	2.5" to 6" (single device) / 6" to 10.1" (dual device) / 10.4" to 15.4" (quad device)
Columns, rows	Up to 129 rows and columns with a maximum of 64 rows and 81 columns (see main configurations in Figure 2)
Interface	I ² C, SPI, UART and USB
Supply voltage range	2.4 to 3.6 V
Max. temperature range	-40 °C to +85 °C
Package	UFBGA 144 (7 x 7 mm, 0.5 pitch) ECOPACK® package

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1 Description

1.1 Device overview

The STM32TS60 product is a multitouch controller device based on Stantum's patented digital resistive multitouch technology. This technology employs the connectivity power of the universal serial bus (USB) with Cortex™-M3 processors and ARM architecture.

Conventional resistive touch controllers are unable to detect more than one contact at a time. Thanks to the STM32TS60 device, it is possible to detect and track up to ten contacts over a touchpanel. The STM32TS60 delivers an exact image of what is happening on the touchpanel surface in the most reliable way with very fast response time and with high noise immunity performances.



1.2 Main benefits

The STM32TS60 represents a breakthrough over competing technologies, bringing outstanding multitouch performance with the best power budget.

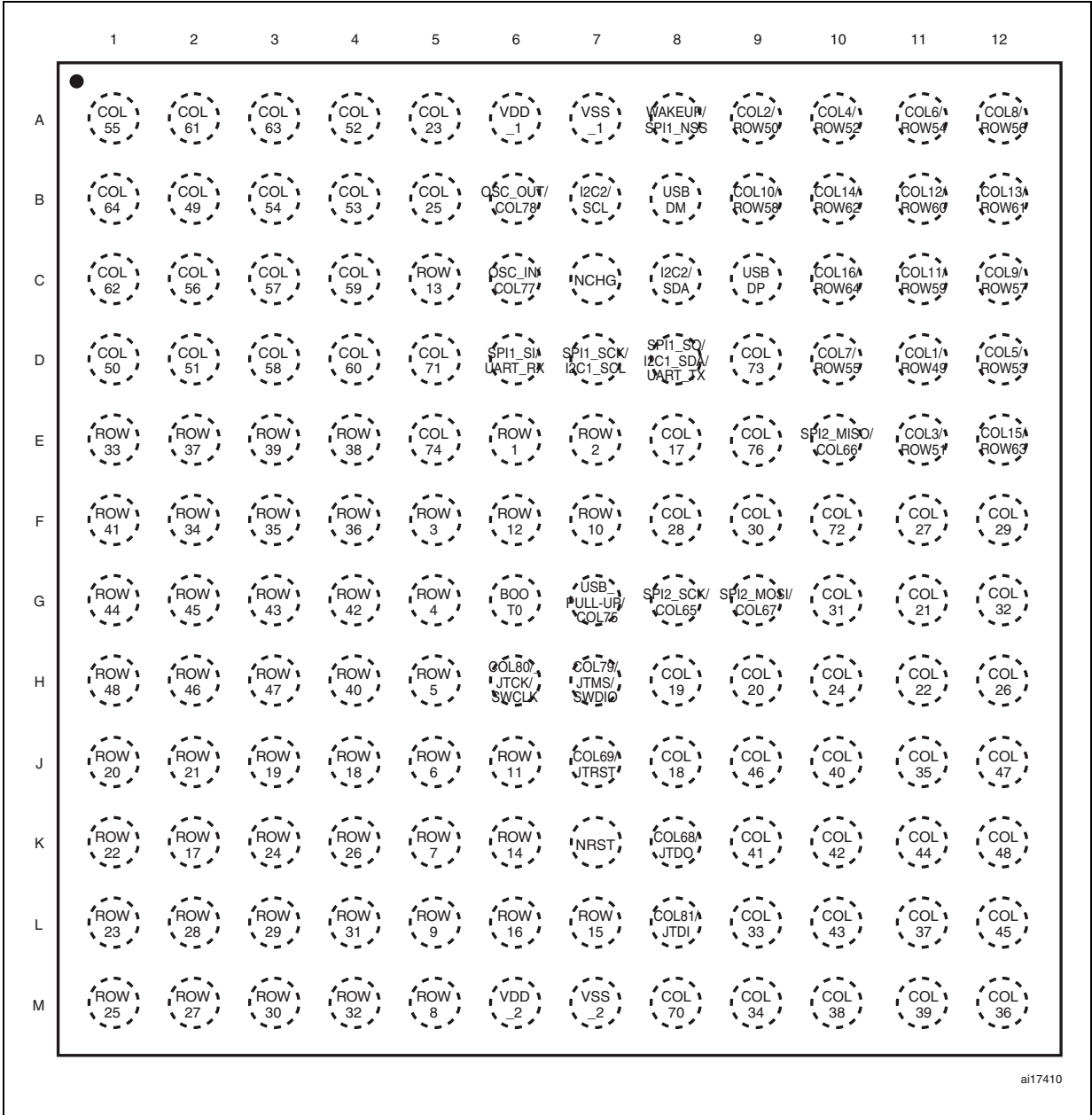
The resistive technology does not require any panel scan during Standby. Consequently, the STM32TS60 device has very low standby power consumption. In addition, this device benefits from the industry-leading mW/MIPS power performance of the ARM Cortex-M3 core.

1.3 Other benefits

- Unique resistive true multitouch technology with up to 10 touches at a time
- Finger, nail and any stylus touch capability
- Fingers actuation force detection based on linear measurement of the touch area surface variation
- High responsiveness with low power consumption (at standby, near zero consumption)
- Homogeneous sensitivity on all points of the touchpanel area
- No calibration
- IP protected by solid patents based on proven resistive technology with very powerful EMI (electromagnetic insulation).
- Very low power Standby mode and zero power resistive panel
- Panel adapted from the proven high-volume resistive technology; able to reach high durability and 90 % transparency.

2 Ballout and pin description

Figure 1. STM32TS60 device UFBGA144 ballout



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Table 2. STM32TS60 pin definitions

Pin no.	Pin type ⁽¹⁾	Pin level ⁽²⁾	Pin name	Pin function
A1	O		COL55	Touchpanel column 55
A2	O		COL61	Touchpanel column 61
A3	O		COL63	Touchpanel column 63
A4	O		COL52	Touchpanel column 52
A5	O		COL23	Touchpanel column 23
A6	S		VDD_1	Supply voltage pin 1
A7	S		VSS_1	Ground pin 1
A8	I		WAKEUP/SPI1_NSS	Device wakeup capability. SPI1 slave select (active low) for host controller communication.
A9	IO		COL2/ROW50	Touchpanel column 2 Touchpanel row 50
A10	IO		COL4/ROW52	Touchpanel column 4 Touchpanel row 52
A11	IO		COL6/ROW54	Touchpanel column 6 Touchpanel row 54
A12	IO		COL8/ROW56	Touchpanel column 8 Touchpanel row 56
B1	O		COL64	Touchpanel column 64
B2	O		COL49	Touchpanel column 49
B3	O		COL54	Touchpanel column 54
B4	O		COL53	Touchpanel column 53
B5	O		COL25	Touchpanel column 25
B6	O		OSC_OUT/COL78	Crystal/resonator oscillator output Touchpanel column 78
B7	OD	FT	I2C2_SCL ⁽³⁾	I ² C2 clock to Haptic system
B8	IO		USBDM	USB data for host controller communication
B9	IO		COL10/ROW58	Touchpanel column 10 Touchpanel row 58
B10	IO		COL14/ROW62	Touchpanel column 14 Touchpanel row 62
B11	IO		COL12/ROW60	Touchpanel column 12 Touchpanel row 60
B12	IO		COL13/ROW61	Touchpanel column 13 Touchpanel row 61
C1	O		COL62	Touchpanel column 62
C2	O		COL56	Touchpanel column 56

Table 2. STM32TS60 pin definitions (continued)

Pin no.	Pin type ⁽¹⁾	Pin level ⁽²⁾	Pin name	Pin function
C3	O		COL57	Touchpanel column 57
C4	O		COL59	Touchpanel column 59
C5	IO		ROW13	Touchpanel row 13
C6	I		OSC_IN/COL77	Crystal/resonator oscillator input Touchpanel column 77
C7	IO	FT	NCHG	Touchpanel change output (active low)
C8	OD		I2C2_SDA ⁽³⁾	I ² C2 data to Haptic system
C9	IO		USBDP	USB data+ for host controller communication
C10	IO		COL16/ROW64	Touchpanel column 16 Touchpanel row 64
C11	IO		COL11/ROW59	Touchpanel column 11 Touchpanel row 59
C12	IO		COL9/ROW57	Touchpanel column 9 Touchpanel row 57
D1	O		COL50	Touchpanel column 50
D2	O		COL51	Touchpanel column 51
D3	O		COL58	Touchpanel column 58
D4	O		COL60	Touchpanel column 60
D5	IO		COL71	Touchpanel column 71
D6	I/I		SPI1_SI/UART_RX	SPI1 slave in for host controller communication. UART data receive for host controller communication.
D7	I/OD	FT	SPI1_SCK/I2C1_SCL	SPI1 clock input for host controller communication. I ² C1 clock input for host controller communication.
D8	O/OD/O	FT	SPI1_SO/I2C1_SDA/UART_TX	SPI1 slave out for host controller communication. I ² C1 data for host controller communication. UART data transmit to host controller.
D9	IO		COL73	Touchpanel column 73
D10	IO		COL7/ROW55	Touchpanel column 7 Touchpanel row 55
D11	IO		COL1/ROW49	Touchpanel column 1 Touchpanel row 49
D12	IO		COL5/ROW53	Touchpanel column 5 Touchpanel row 53
E1	IO		ROW33	Touchpanel row 33

Table 2. STM32TS60 pin definitions (continued)

Pin no.	Pin type ⁽¹⁾	Pin level ⁽²⁾	Pin name	Pin function
E2	IO		ROW37	Touchpanel row 37
E3	IO		ROW39	Touchpanel row 39
E4	IO		ROW38	Touchpanel row 38
E5	IO		COL74	Touchpanel column 74
E6	IO		ROW1	Touchpanel row 1
E7	IO		ROW2	Touchpanel row 2
E8	O		COL17	Touchpanel column 17
E9	O		COL76	Touchpanel column 76
E10	IO/O		SPI2_MISO ⁽⁴⁾ /COL66	SPI2 master in/slave out from/to STMT controller device (extension interface). Touchpanel column 66.
E11	IO		COL3/ROW51	Touchpanel column 3 Touchpanel row 51
E12	IO		COL15/ROW63	Touchpanel column 15 Touchpanel row 63
F1	IO		ROW41	Touchpanel row 41
F2	IO		ROW34	Touchpanel row 34
F3	IO		ROW35	Touchpanel row 35
F4	IO		ROW36	Touchpanel row 36
F5	IO		ROW3	Touchpanel row 3
F6	IO		ROW12	Touchpanel row 12
F7	IO		ROW10	Touchpanel row 10
F8	O		COL28	Touchpanel column 28
F9	O		COL30	Touchpanel column 30
F10	IO		COL72	Touchpanel column 72
F11	O		COL27	Touchpanel column 27
F12	O		COL29	Touchpanel column 29
G1	IO		ROW44	Touchpanel row 44
G2	IO		ROW45	Touchpanel row 45
G3	IO		ROW43	Touchpanel row 43
G4	IO		ROW42	Touchpanel row 42
G5	IO		ROW4	Touchpanel row 4
G6	I		BOOT0	
G7	O		USB_PULL-UP/COL75	USB pull-up control Touchpanel column 75

Table 2. STM32TS60 pin definitions (continued)

Pin no.	Pin type ⁽¹⁾	Pin level ⁽²⁾	Pin name	Pin function
G8	IO/O		SPI2_SCK ⁽⁴⁾ /COL65	SPI2 clock output/input from/to STMT controller device (extension interface). Touchpanel column 65.
G9	IO/O		SPI2_MOSI ⁽⁴⁾ /COL67	SPI2 master out/slave in from/to STMT controller device (extension interface). Touchpanel column 67
G10	O		COL31	Touchpanel column 31
G11	O		COL21	Touchpanel column 21
G12	O		COL32	Touchpanel column 32
H1	IO		ROW48	Touchpanel row 48
H2	IO		ROW46	Touchpanel row 46
H3	IO		ROW47	Touchpanel row 47
H4	IO		ROW40	Touchpanel row 40
H5	IO		ROW5	Touchpanel row 5
H6	I/O		COL80/JTCK/SWCLK	Touchpanel column 80 JTAG clock Serial wire clock
H7	I/O		COL79/JTMS/SWDIO	Touchpanel column 79 JTAG mode selection Serial wire data input/output
H8	O		COL19	Touchpanel column 19
H9	O		COL20	Touchpanel column 20
H10	O		COL24	Touchpanel column 24
H11	O		COL22	Touchpanel column 22
H12	O		COL26	Touchpanel column 26
J1	IO		ROW20	Touchpanel row 20
J2	IO		ROW21	Touchpanel row 21
J3	IO		ROW19	Touchpanel row 19
J4	IO		ROW18	Touchpanel row 18
J5	IO		ROW6	Touchpanel row 6
J6	IO		ROW11	Touchpanel row 11
J7	IO		COL69/JTRST	Touchpanel column 69 JTAG reset
J8	O		COL18	Touchpanel column 18
J9	O		COL46	Touchpanel column 46
J10	O		COL40	Touchpanel column 40
J11	O		COL35	Touchpanel column 35

Table 2. STM32TS60 pin definitions (continued)

Pin no.	Pin type ⁽¹⁾	Pin level ⁽²⁾	Pin name	Pin function
J12	O		COL47	Touchpanel column 47
K1	IO		ROW22	Touchpanel row 22
K2	IO		ROW17	Touchpanel row 17
K3	IO		ROW24	Touchpanel row 24
K4	IO		ROW26	Touchpanel row 26
K5	IO		ROW7	Touchpanel row 7
K6	IO		ROW14	Touchpanel row 14
K7	IO		NRST	Reset (active low)
K8	O/O		COL68/JTDO	Touchpanel column 68 JTAG data output
K9	O		COL41	Touchpanel column 41
K10	O		COL42	Touchpanel column 42
K11	O		COL44	Touchpanel column 44
K12	O		COL48	Touchpanel column 48
L1	IO		ROW23	Touchpanel row 23
L2	IO		ROW28	Touchpanel row 28
L3	IO		ROW29	Touchpanel row 29
L4	IO		ROW31	Touchpanel row 31
L5	IO		ROW9	Touchpanel row 9
L6	IO		ROW16	Touchpanel row 16
L7	IO		ROW15	Touchpanel row 15
L8	IO		COL81/JTDI	Touchpanel column 81 JTAG data input
L9	O		COL33	Touchpanel column 33
L10	O		COL43	Touchpanel column 43
L11	O		COL37	Touchpanel column 37
L12	O		COL45	Touchpanel column 45
M1	IO		ROW25	Touchpanel row 25
M2	IO		ROW27	Touchpanel row 27
M3	IO		ROW30	Touchpanel row 30
M4	IO		ROW32	Touchpanel row 32
M5	IO		ROW8	Touchpanel row 8
M6	S		VDD_2	Supply voltage pin 2
M7	S		VSS_2	Ground pin 2
M8	IO		COL70	Touchpanel column 70

Table 2. STM32TS60 pin definitions (continued)

Pin no.	Pin type ⁽¹⁾	Pin level ⁽²⁾	Pin name	Pin function
M9	O		COL34	Touchpanel column 34
M10	O		COL38	Touchpanel column 38
M11	O		COL39	Touchpanel column 39
M12	O		COL36	Touchpanel column 36

1. I = input pin, O = output push-pull, IO = input/output, OD = output open drain, S = supply pin

2. FT = 5 V tolerant

3. I²C2 interface is designed to drive an Haptic system

4. SPI2 is used to interconnect the STMT controller for multidevice systems.

3 Application diagrams

Figure 2. Single-device typical application schematic for 2.5" to 6" panels

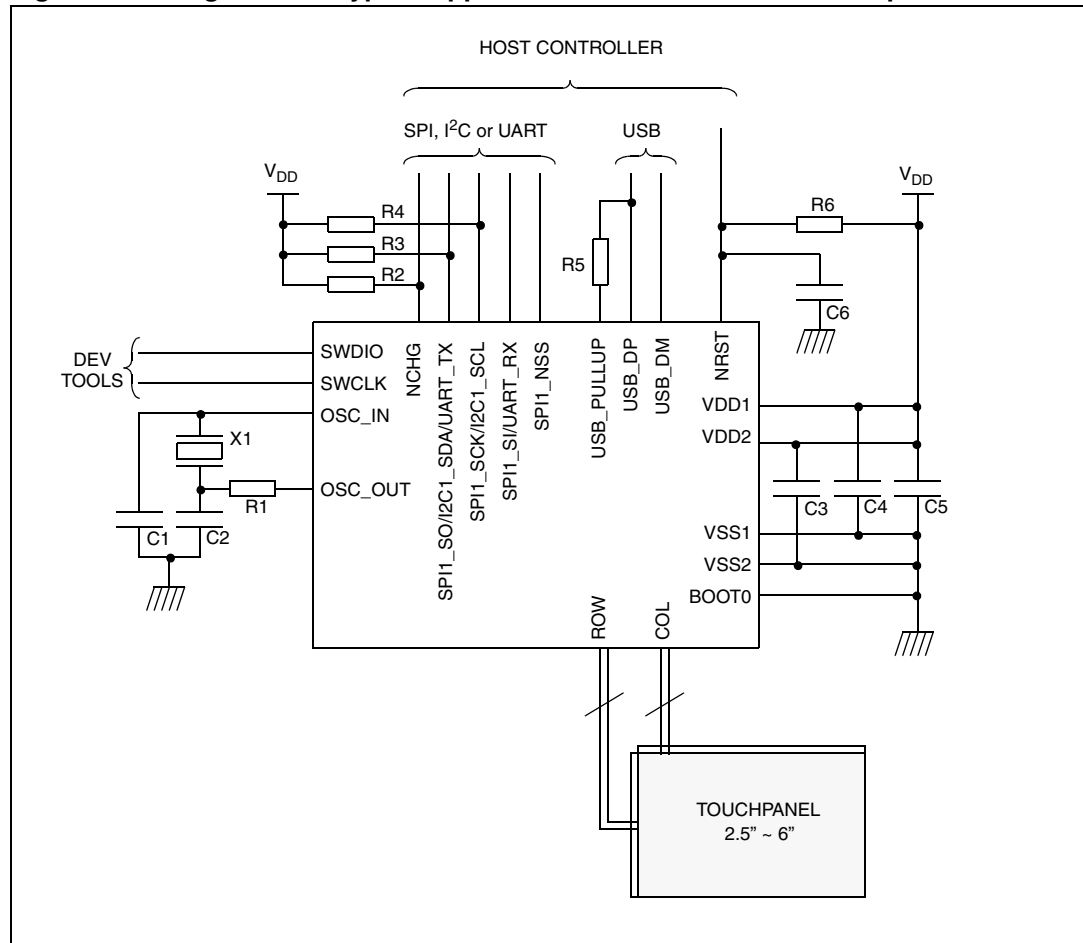


Table 3. Single-device typical application passive component list

Ref.	Typ. Value	Comment	Ref.	Typ. value	Comment
C1,C2	18 pF	For USB interface only	C3,C4	100 nF	Decoupling capacitors
X1	16 MHz	For USB interface only	C5	1 µF	Filtering capacitors
R1	(1)	For USB interface only	C6	10 nF	Reset filter
R2	10 KΩ		R5	1.5 KΩ	For USB interface only
R3,R4	4.7 KΩ	For I²C interface only	R6	10 KΩ	Reset filter

1. Value depends on resonator or crystal R_S resistance.

Figure 3. Dual-device typical application schematic for 6" to 10.1" panels

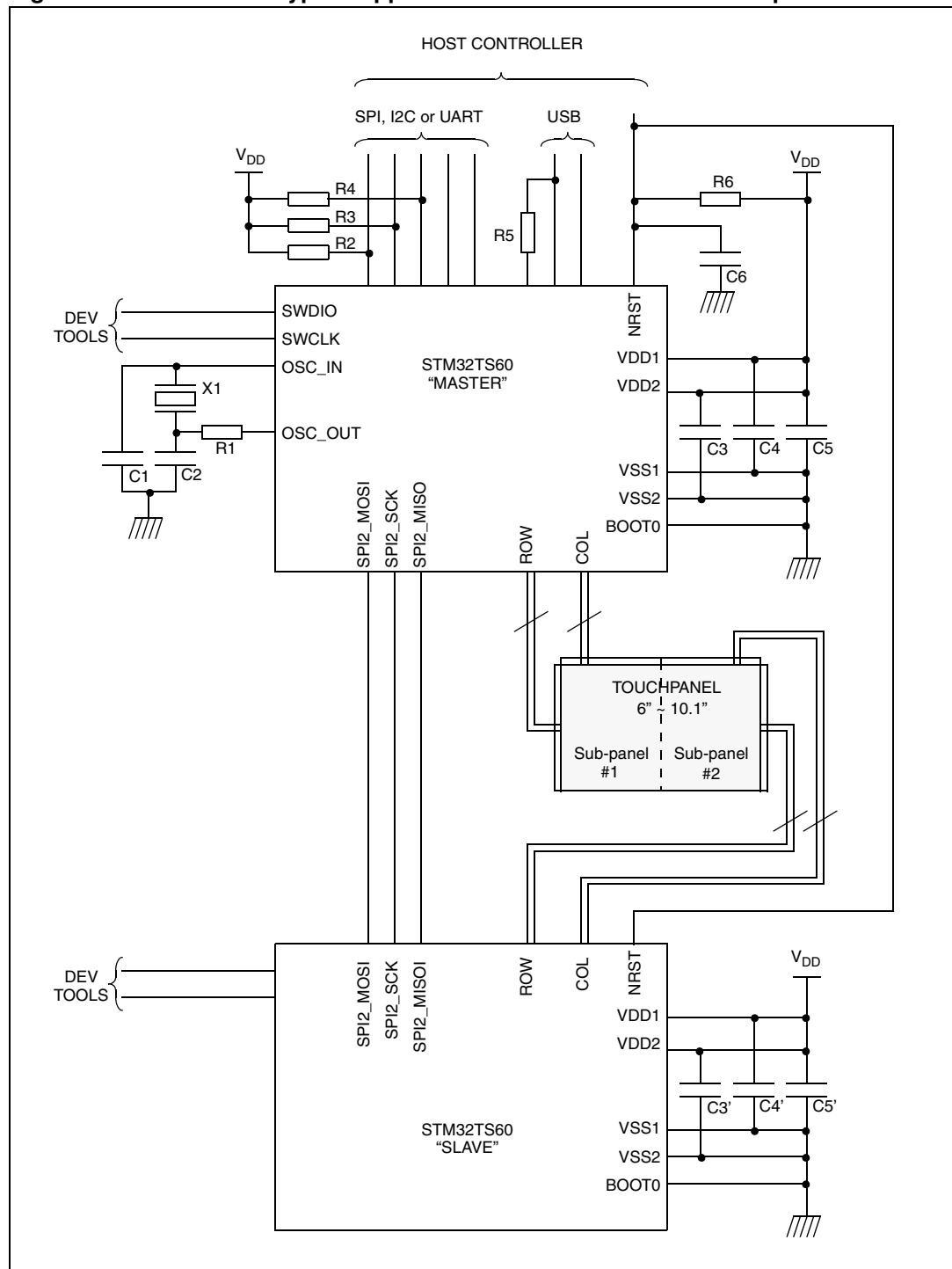


Table 4. Dual-device typical application passive component list

Ref.	Typ. value	Comment	Ref.	Typ. value	Comment
C1,C2	18 pF	For USB interface only	C3,C4,C3',C4'	100 nF	Decoupling capacitors
X1	16 MHz	For USB interface only	C5, C5'	1 μ F	Filtering capacitors
R1	— ⁽¹⁾	For USB interface only	C6	10 nF	Reset filter
R2	10K Ω		R5	1.5 K Ω	For USB interface only
R3,R4	4.7K Ω	For I ² C interface only	R6	10 K Ω	Reset filter

1. Value depends on resonator or crystal R_S resistance.

4 Part numbering

Table 5. Ordering information scheme

Example:	STM32	TS	60	Z	H	6	xx	y
Device family								
STM32 = ARM-based 32-bit microcontroller								
Device sub-family								
TS = touchscreen family								
Touch sensing technology								
60 = multitouch resistive								
Pin count								
Z = 144 pins								
Package								
H = UFBGA								
Temperature range								
6 = industrial temperature range –40°C to 85°C								
Firmware configuration								
Firmware revision								

For further information on any aspect of this device, please contact your nearest ST Sales Office.

The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.



5 Revision history

Table 6. Document revision history

Date	Revision	Changes
16-Dec-2009	1	Initial release

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